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DATE: September 16, 2005

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\*\*\*\*\*Docket No.: SC12865TH  
Applicant: Afzal Malik et al.  
Serial No.: 10/600,959  
Art Unit: 2189  
Filed: June 20, 2003

## ALL ITEMS MARKED WITH AN "X" ARE INCLUDED:

1.	x	1 page Facsimile Cover Sheet
2	x	3 page Reply Brief Under 35 C.F.R. 1.193(b)(1)

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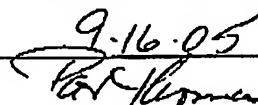
## UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT Afzal Malik et al. GROUP ART UNIT: 2189  
APPLN. NO.: 10/600,959 EXAMINER: Christian Chace  
FILED: June 20, 2003 CONFIRMATION No.: 6580  
TITLE: METHOD AND APPARATUS FOR DYNAMIC PREFETCH  
BUFFER CONFIGURATION AND REPLACEMENT

Certificate of Transmission under 37 C.F.R. 1.8

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## REPLY BRIEF UNDER 37 C.F.R. 1.193(b)(1)

COMMISSIONER FOR PATENTS  
ALEXANDRIA, VA 22313

An Examiner's answer to Applicants' Appeal Brief was mailed on September 9, 2005. In response, Applicants are herein filing a reply brief. Applicants thank each of the three examiners who signed the Examiner's answer for their time and reasoned response.

In response to the stated reasons for rejection of claims 1-6, 8-10, 13-16 and 19 under 35 U.S.C. 102(e), Applicants respectfully submit that claim recitals in each of the independent claims are not taught by the relied upon reference Peters (U.S. Patent 6,636,927). In claim 1, Peters does not teach the recited "the prefetch buffer having lines of differing total length during operation". Peters uses a prefetch buffer having fixed length lines that are master specific as clearly shown in Figure 7 of Peters and described from Col. 9, line 56 to Col. 10, line 20. The Peters reference teaches, as the title states, the transferring of data using master-specific prefetch

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sizes. Peters uses a control register to control the reading of differing amounts of data from a fixed length buffer line. When the F0 field of control register 308 of Figure 6 controls, less than all of a line of data from the prefetch data is read (Col. 9, lines 32-34). Therefore, a portion of the prefetch buffer line becomes unused. Peters does not teach the claim 1 recital "eliminating dedication of buffer storage to unused portions of the one or more prefetch buffer lines" and this claim recital is not inherent as stated on page 12 of the Examiner's answer. These claim 1 features do not boil down to claim interpretation as stated in the Appeal Brief. There is no teaching or suggestion by Peters of those features. The reading of differing amounts of data from a prefetch buffer having line lengths that remain fixed taught by Peters is readily distinguishable from the clear meaning of the language of claim 1.

With respect to the claim 1 recital "selectively modifying total length of one or more prefetch buffer lines of the prefetch buffer", the Peters system modifies the amount of data that is read from a prefetch buffer having fixed size lines. The difference between modifying a line length versus modifying an amount of data read from a fixed size line length is not a matter of claim interpretation, and this functional difference is clearly present in claim 1. Peters teaches that the control register is programmable for flexibility in changing the amount of data that is read from the prefetch buffer. This programmable feature in the Peters system does not adjust the number of bits associated with a line in the buffer, and there remain unused portions of a buffer line when the control register indicates to read less than an entire line.

In claim 14, Peters does not teach "selectively modifying total length of the replacement entry of the prefetch buffer based on an attribute of the read request to an adjusted line size that eliminates dedicating unused buffer storage to the replacement entry of the prefetch buffer". The Peters system uses a control register to vary the percentage of data that is read from a fixed size buffer line. When less than an entire line is read, as controlled in Figure 6 by Field F0, unused buffer storage exists in the form of the remainder of the line that is not read. The claimed distinguishing features permit a prefetch buffer to be efficiently organized into lines of varying

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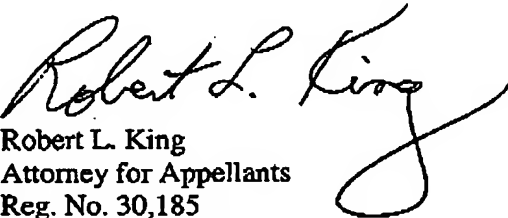
sizes to avoid dedicating one prefetch buffer line to a specific master's size. Thus significantly more efficient use of memory storage is provided.

These distinctions in independent claims 1 and 14 are consistent with what Applicants have previously advocated, and the positions with illustrative advantages that Applicants have stated in the Brief and this Reply Brief are commensurate in scope with the claim language.

With respect to the 35 U.S.C. 103(a) rejection of dependent claims 17 and 18, the Examiner's Answer was a reference to the body of the final rejection response. Accordingly, the prior record adequately addresses the issues and positions.

No fee is believed owed as a result of this communication.

Respectfully submitted,  
AFZAL MALIK et al.



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